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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,206	11/26/2003	Michael A. Gaynes	FR920030002US1	1205

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,206	GAYNES ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *14-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-13 in the reply filed on October 19, 2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Terui (US 6225694).

Regarding claim 1, Fig. 1 of Terui shows a semiconductor package comprising: a chip carrier [1] including a grounded pad [a conductive layer underneath the layer 4] on a first side of said chip carrier;

a semiconductor chip [12] coupled to said first side of said chip carrier;

a conductive lid [15; a metal cap] thermally coupled to said semiconductor chip; and a conductive structure [4] electrically coupled to said grounded pad and to said conductive lid (col. 2, lines 20-25 and col. 2, lines 59-68).

Regarding claim 2, Fig. 1 of Terui shows a solder [16, col. lines 52-54] connects said conductive structure and said grounded pad.

Regarding claim 3, Fig. 1 of Terui shows that said conductive structure is electrically coupled to said grounded pad with an electrically conductive adhesive

material [16; anisotropic conductive adhesive; col. 2, lines col. lines 52-54].

Regarding claim 4, Fig. 1 of Terui shows said conductive structure is electrically coupled to said conductive lid with an electrically conductive adhesive material [16; anisotropic conductive adhesive; col. 2, lines col. lines 52-54].

Regarding claim 8, Fig. 2B of Terui shows said conductive structure [4] comprises a block.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-6, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terui in view of Mertol (US 5866943).

Regarding claim 5, Fig. 1 of Terui shows substantially the entire claimed structure except "said conductive structure is coupled to said chip carrier using an electrically insulative adhesive material." Fig. 3 of Mertol shows a semiconductor wherein a conductive structure [24] is coupled to said chip carrier [22] using an electrically insulative adhesive material (col. 8, lines 59-64). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mertol into the device of Terui in order to have the conductive structure coupled to said chip carrier using an electrically insulative adhesive material to prevent possible short circuits.

Regarding claim 6, Fig. 1 of Terui shows substantially the entire claimed structure except "said conductive structure is coupled to said chip carrier using a thermally conductive adhesive material." Fig. 3 of Mertol shows a semiconductor wherein a conductive structure [24] is coupled to said chip carrier [22] using a thermally conductive adhesive material (col. 8, lines 59-64). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mertol into the device of Terui in order to have the conductive structure coupled to said chip carrier using a thermally conductive adhesive material to enhance heat dissipation.

Regarding claim 10, Fig. 1 of Terui shows substantially the entire claimed structure including a solder [16] couples said conductive structure to said grounded pad, however, fails to show "an electrically conductive adhesive material couples said conductive structure to said conductive lid; and an electrically insulative adhesive material couples said conductive structure to the chip carrier." Fig. 3 of Mertol shows a semiconductor wherein an electrically conductive adhesive material [42; col.10, lines 22-25] couples said conductive structure [24] to a conductive lid [26] and an electrically insulative adhesive material couples [36; col. 8, lines 59-64] said conductive structure to a chip carrier [22]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Mertol into the device of Terui in order to have an electrically conductive adhesive material coupling the conductive structure to the conductive lid for grounding effect and an electrically insulative adhesive material coupling the conductive structure to a chip carrier for prevention of short circuits.

Regarding claim 12, Fig. 2B of Terui shows said conductive structure [4] comprises a block.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terui in view of Glenn et al. (US 6562655), hereinafter Glenn.

Regarding claim 7, Fig. 1 of Terui shows substantially the entire claimed structure except "said conductive structure comprises a spring." Fig. 6 of Glenn shows a semiconductor with a conductive structure comprising a spring [150]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Glenn into the device of Terui in order to have a conductive structure comprising a spring to secure the conductive lid.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terui in view of Hoffman (US *6630661).*

Regarding claim 9, Fig. 1 of Terui shows substantially the entire claimed structure except "said block comprises a surface mount technology (SMT) discrete component." Fig. 7 of Hoffman shows a semiconductor with a block comprising a surface mount technology (SMT) discrete component [154; col. 6, lines 47-50] It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hoffman into the device of Terui in order to have semiconductor device with a block comprising a surface mount technology (SMT) discrete component to form an IC.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terui and Mertol as applied to claim 10 above, and further in view of Glenn.

Regarding claim 11, the combined teachings of Terui and Mertol show most aspect of the instant invention except "said conductive structure comprises a conductive spring." Fig. 6 of Glenn shows a semiconductor with a conductive structure comprising a conductive spring [150]. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Glenn into the device of Terui and Mertol in order to have a conductive structure comprising a conductive spring to secure the conductive lid.

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Terui and Mertol as applied to claim 10 above, and further in view of Hoffman.

Regarding claim 13, the combined teachings of Terui and Mertol show most aspect of the instant invention except "said block comprises a surface mount technology (SMT) discrete component." Fig. 7 of Hoffman shows a semiconductor with a block comprising a surface mount technology (SMT) discrete component [154; col. 6, lines 47-50] It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hoffman into the device of Terui and Mertol in order to have semiconductor device with a block comprising a surface mount technology (SMT) discrete component to form an IC.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi

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SUPERVISORY PATENT EXAMINER
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